Claims

[c1] What is claimed is:

1.A mux scan cell comprising:

a multiplexer comprising:

a first input node for receiving raw data;

a second input node for receiving test data;

an output node for outputting data;

a selection node for selecting an input from the first input node or the second input node; and

a delay circuit electrically connected between the second input node and the output node for prolonging a traveling time which the test data takes to travel from the second input node to the output node; and

a flip-flop connected to the output node of the multiplexer;

wherein the traveling time of the test data is prolonged such that the traveling time which the test data takes to travel from the second input node to the output node simulates a sum of a traveling time in which the raw data travels through a combinational logic and a traveling time in which the raw data travels from the first input node to the output node.

[c2] 2.The mux scan cell of claim 1 being a mux scan cell of a plurality of sequentially connected mux scan cells which form a mux scan chain.

[c3] 3.The mux scan cell of claim 2 wherein the flip-flop of the mux scan cell is electrically connected to a multiplexer of a following mux scan cell.

[c4] 4.The mux scan cell of claim 1 wherein the delay circuit of the multiplexer comprises a delay buffer.

[c5] 5.The mux scan cell of claim 1 wherein the delay circuit of the multiplexer comprises an RC circuit.

[c6] 6.The mux scan cell of claim 1 wherein the delay circuit of the multiplexer comprises a narrow width transistor.

[c7] 7.The mux scan cell of claim 1 wherein the delay circuit of the multiplexer comprises a wire delay.